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# Engineering Note

**Date:** July 21,1998
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**Project:** CFT Axial Trigger Board
**Doc. No:** A980721A

**Subject:** Purported Schedule Guesstimate

According to information provided by other members of the CFT project team, the end goal of the current development is to produce a prototype CFT Axial Trigger card by sometime in December, 1998. This document will try to work backwards from that date to determine probable "drop dead" dates for various major decisions within the project.

## *Board Test and Assembly*

It's not unreasonable to ask for a few weeks to test the board after delivery. Also, at least a week and probably two should be allocated for stuffing the board with parts once it's received. The combination of these factors sets the latest date at which the PC board and all parts arrive at D-Zero to approximately 11/13/98. This date – seven weeks prior to end of year – allows for for three weeks of board test time between the Thanksgiving holiday and the Christmas Lab shutdown, plus 1 ½ weeks for stuffing the PC board after delivery.

## *PCB Delivery Path*

Working backwards from 11/13/98, the following variables need be considered for the PCB itself:

- PCB Vendor turnaround time. Three weeks ARO is fairly standard.
- Local FNAL delay from submission of purchase request to placement of purchase order. Again, three weeks is not unreasonable, and in fact may be asking for speed. It depends on the local approval path.
- PCB layout will probably take four weeks. The presumption is that the PCB layout will be done off-site, so another purchasing delay cycle means that a requisition to purchase the PCB layout services has to be done four weeks before the layout service starts work.
- Schematic entry will probably take three weeks.

These estimates yield the following dates:

- A requisition to the PCB layout vendor need be placed by 8/7/98.
- A requisition to the PCB manufacturer need be placed by 9/25/98.
- The design must be specified fully enough for schematic entry to begin no later than 8/14/98. ***This includes sufficient specification of the FPGA/CPLD devices as discussed below.***

## *Parts Procurement*

A similar backwards timeline may be used to work out parts choices.

- Parts delivery can often be very long due to shortages or lack of priority. FNAL orders are often small with respect to other customers, so we sometimes move to the bottom of the heap. To be conservative, I've estimated that it will take 11 weeks ARO to get the parts.
- As always, I estimate four weeks from when you write the req to when the order is actually placed.

- This means that the FPGA/PLD components used in the board must be decided upon by no later than 7/31/98. This allows four weeks from the date in which the devices are chosen to do the internal design and pin fixing for entry into the schematic during the last week of schematic entry.

Note that the FPGA/PLD decision affects not only the timeline for parts procurement, but also the PCB layout. It's wonderful if the parts will be delivered faster, but that doesn't allow for any slippage in the choice of what parts are used, because that's still on the critical path through the PCB design process.

## *SIFT Test Efforts*

In a similar vein to the PCB design, efforts to build SIFT and MCM test stands need be complete sufficiently before the boards come back to allow the SIFT MCMs to be tested prior to their insertion into the boards. Thus, the MCM test stand needs to be in place by early September, and the time period of September-November is allocated for developing the software which will test the CFT board, SIFTs and all.

## *Graphical View*

Here's a timeline showing how it all fits. We need make decisions, and need to make them NOW.